1 Comparators.

1.1 Definitions

A comparator is a functional block that gets a differential input voltage and produces a digital output signal. If we suppose that the output analog voltages corresponding to logical values "0" and "1" are 0 V and V_{dd},, respectively, the ideal response of a comparator is shown in Fig.1.1 (a).

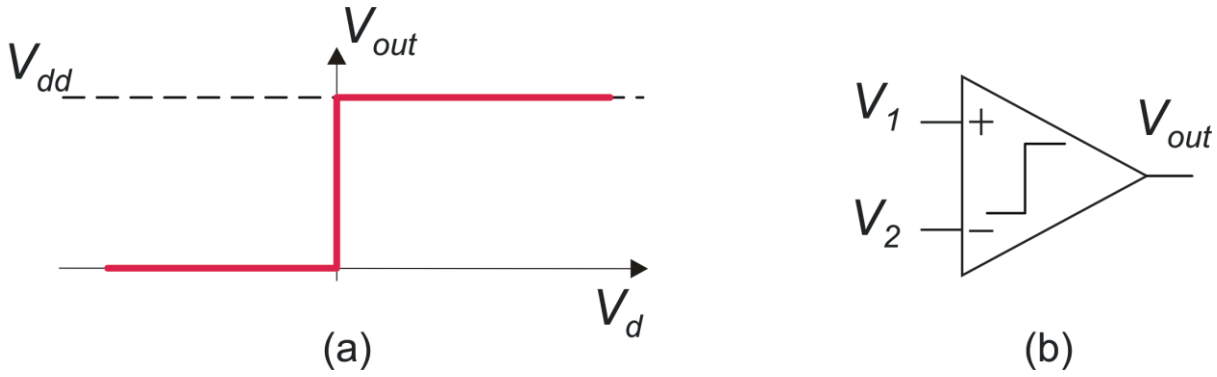

Fig.1.1. (a) Ideal comparator response. (b) Ideal comparator symbol.

The symbol of the ideal comparator is shown in Fig.1.1 (b). Considering the ideal response, V_{out} is "1" if $Vd=V_1-V_2>0$, that is if $V_1>V_2$. For this reason, a comparator can be used to decide whether a Voltage is greater than another one. Comparators are widely used in analog-to-digital converters (ADCs) and waveform generators.

The ideal characteristic of Fig.1.1 (a) can be approximated using a very-high gain amplifier, such as an op-amp. In this case, the real characteristic will look like the curve of Fig.1.2. The drawback of this solution is that the transition between the two logical levels has a finite slope. Thus, there is an interval of differential voltages, which do not produce a valid output logical value.

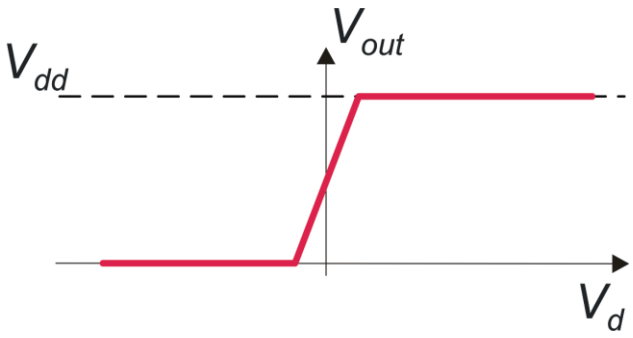

Fig.1.2. Response of a comparator implemented with an high-gain amplifier.

Even if this interval can be made as small as a few microvolts, it can still cause serious problems, such as metastability of the logic blocks that receive the output voltage or unwanted parasitic analog feedback paths that may froze the system in an unpredictable state.

To overcome this problem it is necessary to introduce hysteresis in the comparator response. This is obtained by means of positive feedback (regenerative comparators). A typical response with hysteresis is depicted in Fig.1.3.

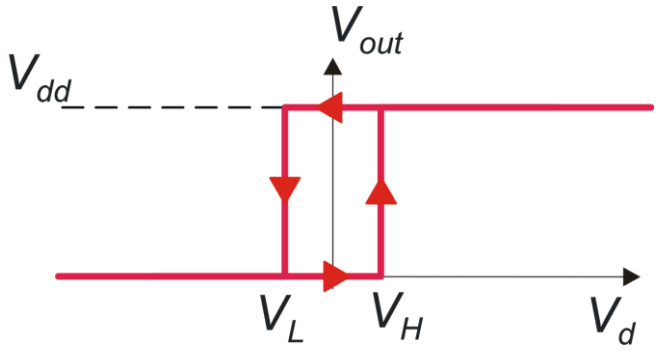

Fig.1.3. Typical behavior of a comparator with hysteresis (regenerative comparator).The segments between V_L and V_H can be traveled only across the direction indicated by the arrows.

If we apply a negative input differential voltage below V_L (lower threshold), V_{out} is always zero. If V_d is progressively increased, V_{out} gets high when V_d overcomes V_H (upper threshold). To set V_{out} back to zero, it is not sufficient to cross V_H backwards, but it is necessary go further and cross V_L. Thus, the dependence of V_{out} on V_d is different if we proceed from lower to higher input differential voltages or vice versa. Note that an input differential voltage between V_L and V_H may produce two different output states, depending on the previous history. Vertical branches are really vertical: once the input voltage reaches one on the two thresholds, V_H (from below) and V_L (from above), the transition is completed by positive feedback with no need of further input signal increase. In this way, there is no risk of having an invalid output logical value. The difference between V_H and V_L is indicates as the hysteresis range (or width):

$$\Delta V_h \equiv V_H - V_L \tag{1.1}$$

1.2 Four transistors hysteresis cell.

By applying positive feedback to an operational amplifier, it is possible to obtain a regenerative comparator. Indicated as Schmitt trigger. This is not an optimum solution for integrated comparators, since it uses a rather complex circuit (the op-amp), requires resistors, and does not have a real differential input. On the other hand, most integrated comparators are based on the four-transistor cell shown in Fig.1.4. Diode-connected MOSFETs M1 and M4 have an aspect ratio indicated with β_L (where the subscript "L" stands for "load"), while M2 and M3 aspect ratio is β_C, (where the subscript "C" recalls their cross-coupled connection). The input signal are the two currents I_1 and I_2, which are such that

$$I_1 + I_2 = I_0 \tag{1.2}$$

The output quantities are voltages V_1 and V_2. In order to understand the behavior of this cell, we will start by considering the case where $I_1=I_0$ and, consequently $I_2=0$. In this condition, since $I_2=I_{D3}+I_{D4}$, and $I_{D3}, I_{D4} \geq 0$, the only possible solution is $I_{D3}=I_{D4}=0$. This means that $V_2<V_t$ and then, M2 and M4 (that share the same $V_{GS}=V_2$) are off.

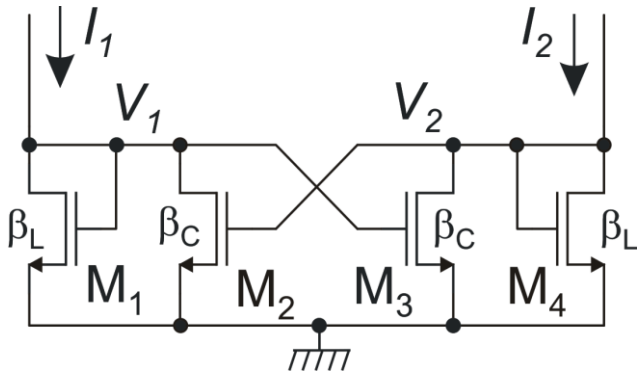

Fig.1.4. Four-transistor hysteresis cell.

If M2 is off, than $I_{D1}=I_1=I_0>0$, thus $V_1>V_t$. Since $V_1=V_{GS1}=V_{GS3}$, then M1 and M3 are both in on-state. Considering that $I_{D3}=0$, it should be $V_{DS3}=V_2=0$. Then we can summarize voltages and currents in this initial state as follows:

$$\text{for } I_1 = I_0,\ I_2 = 0: \begin{cases} M1, M3: on \quad M2, M4: off \\ I_{D1} = I_0, \quad I_{D2} = I_{D3} = I_{D4} = 0 \\ V_2 = 0 \quad V_1 = V_{GS1} > V_t \end{cases} \tag{1.3}$$

The voltage V_1 can be easily calculated considering that $I_{D1}=I_1$ and supposing that M1 operates in strong inversion:

$$V_1 = V_{GS1} = V_t + \sqrt{\frac{2I_1}{\beta_L}} \tag{1.4}$$

For correct operation of the cell the following condition should be fulfilled:

$$V_1 < 2V_t \tag{1.5}$$

The maximum value assumed by V_1 occurs when I_1 is maximum. This occurs in the condition that we have just studied, i.e. when $I_1=I_0$, so that, (1.4) holds true for every I_1 value, if we impose:

$$V_{1\max} = V_t + \sqrt{\frac{2I_0}{\beta_L}} \le 2V_t \quad \Rightarrow \quad \sqrt{\frac{2I_0}{\beta_L}} = \left(V_{GS1} - V_t\right)_{I_{D1}=I_0} < V_t \tag{1.6}$$

This is not a strict requirement, since V_t is generally in the order of several hundred millivolts. The reason to impose condition (1.6) will be clear in the next discussion.

Now, let us start increasing I_2 from its initial zero value. Clearly, due to (1.2), I_1 will decrease accordingly. The increase of I_2 produces an increment of voltage V_2, as shown in Fig.1.5. In practice, for a small I_2 increment, V_2 remains below V_t, so that M4 is still off and I_2 is carried only by M3, so that $I_2= I_{D3}$, In addition, also M2 is still off, so that $I_1=I_{D1}$. The decrease of I_1 make $V_1 = V_{GS1} =V_{GS3}$ decrease through (1.4). Fig. 1.5 clearly shows that both I_2 increase and V_1 decrease contribute to increase V_2.

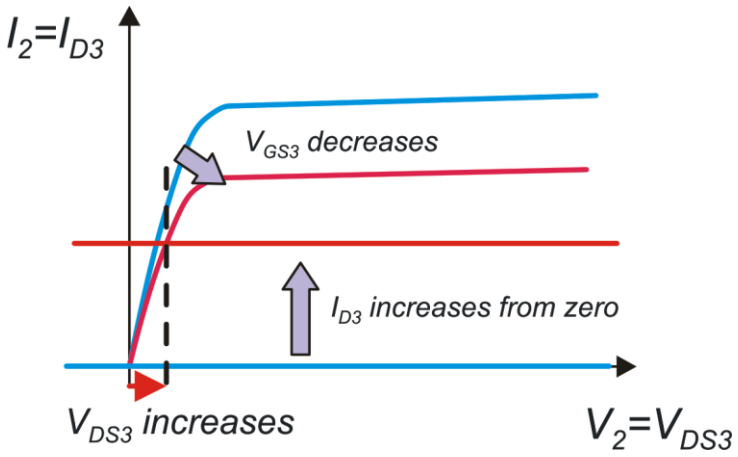

Fig.1.5. M3 output characteristics used to illustrate the effects of an increase if I_2 from the zero initial value.

If I_2 is increased further, V_2 continues to increase and V_1 to decrease. The only active devices continue to be M1 and M3 until V_2 reaches V_t. At this point also M2 and M4 turn on and the situation changes. Let us focus on M2. As soon as M2 starts carrying a non-zero current, it steals current from M1, further reducing I_{D1} and then V_1, through (1.4). Considering Fig.1.5, a V_1 (i.e. V_{GS3}) reduction, cause V_2 to further increase and, in turn, this leads M2 to steal more current from M1. This is clearly a positive feedback mechanism, which, if the loop gain is greater than one, cause instability. In this case, a sharp transition occurs even if current I_2 is not increased further and the state of the cell is flipped. For such an effect to be triggered, it is necessary that V_2 overcome V_t, starting to turn on M2. We can study the cell for a V_2 just equal to V_t, when M2 is still off. Figure 1.6 shows the cell in this condition. MOSFETS drawn in gray are still off.

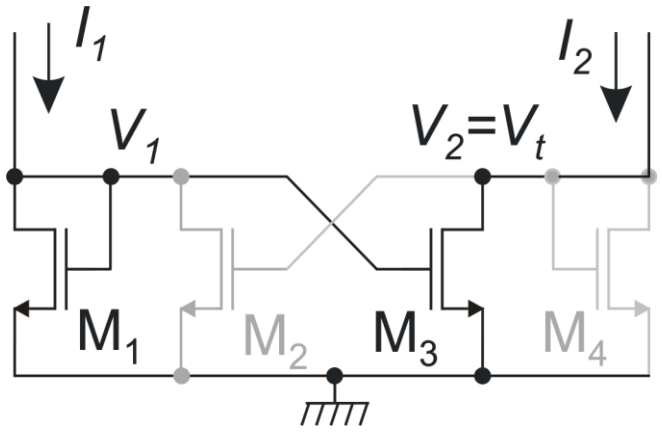

Fig.1.6. Situation before state transition..

Note that M1 and M3 form a current mirror. M1 operates in saturation region, due to its diode-like connection. If also M3 in in saturation, then:

$$\frac{I_2}{I_1}=\frac{I_{D3}}{I_{D1}}=\frac{\beta_C}{\beta_L} \tag{1.7}$$

In order to confirm that M3 actually operates in saturation, we have to verify the usual inequality: $V_{DS3}>V_{GS3}-V_t$. But, for the particular point that we are analyzing, $V_{DS3}=V_2=V_t$. Then, the inequality to verify becomes:

$$V_{GS3} < 2V_t \tag{1.8}$$

Since $V_{GS3} = V_1$, condition (1.5), which we have imposed by design, guarantees that (1.8) holds true, thus confirming that M3 is in saturation when V_2 reaches the threshold V_t. Note that when I_2 is zero or much smaller than I_1 (as at the beginning of our analysis), V_2 (i.e. V_{DS3}) is so small that M3 is in triode region. As I_2 is progressively increase, M_3 passes from triode to saturation. When this occurs, a very small I_2 increase produces a large V_2 increase (due to the high output resistance exhibited in saturation) so that the condition $V_2=V_t$ is reached with no need of increasing I_2 much further.

Now consider (1.7). If we design the circuit imposing the following condition:

$$r_h \equiv \frac{\beta_C}{\beta_L} > 1, \tag{1.9}$$

voltage V_2 reaches V_t and then starts the transition when $I_2/I_1 >1$, thus when we have passed the point marked by $I_1=I_2=I_0/2$. The situation is depicted in the plot of Fig.1.7, where we are showing the behavior of V_1 and V_2 up to the transition.

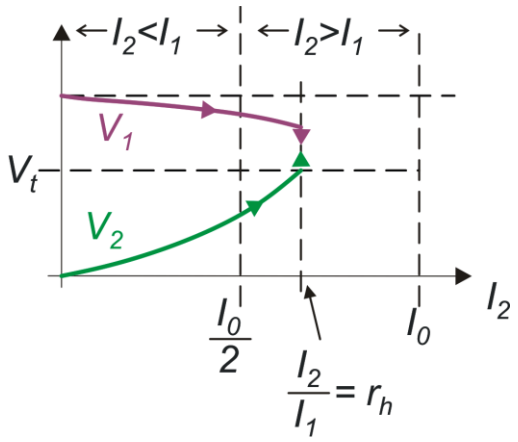

Fig.1.7. Behavior of V_1 and V_2 from the case $I_2=0$ to the transition.

If the I_2/I_1 ratio is increased over r_h, the cited positive feedback mechanism makes V_2 and V_1 swap, as indicated by the arrows. In order to determine the behavior for $I_2/I_1 > r_h$, we have to repeat the same considerations made so far, but starting from the opposite condition, i.e. $I_1=0$, $I_2=I_0$. Due to the symmetry of the cell, we will obtain the behavior shown in Fig. 1.8.

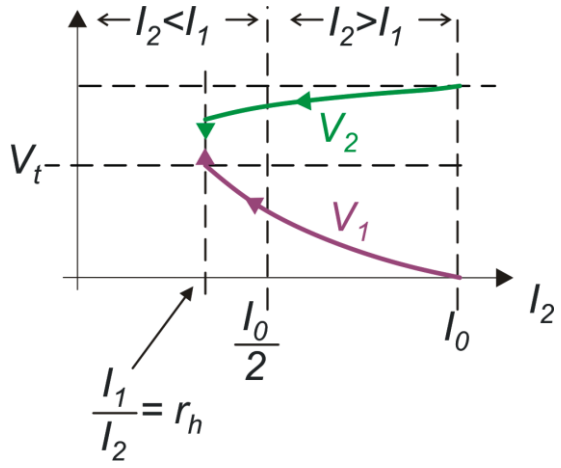

Fig.1.8. Behavior of V_1 and V_2 from the case I_2=0 to the transition.

Since the behavior should be symmetrical to the case of Fig.1.7, the transition will occur for $I_1 > I_2$ (i.e. $I_2/I_1 < 1$. Thus, the transition occurs at different I_2/I_1 ratio depending on which one of the extreme conditions I_2=0 or I_1=0 we start from. Comparing Fig.1.7 and 1.8, we note that, for:

$$\frac{1}{r_h} < \frac{I_2}{I_1} < r_h, \tag{1.10}$$

there are two possible solutions for V_1 and V_2, depending on whether we started from I_2=0 (i.e. from the left of the diagram) or from I_2=I_0 (i.e. from the right). This a clear indication of the presence of the hysteresis.

Furthermore, if we consider again the first case that we have analyzed, depicted in Fig.1.9, we can now understand what happens for $I_2/I_1 > r_h$. In this region, a solution for V_1 and V_2 is given by the curves of Fig.1.7. So if I_2 is increased beyond the transition, the curves of Fig. 1.7 join the corresponding curves of Fig.1.8. The result is shown in Fig. 1.9 (a), which represents the complete behavior of the cell when I_2 is progressively increased from 0 to I_0. The opposite case, obtained decreasing I_2 from I_0 to 0 is shown in Fig.1.9 (b).

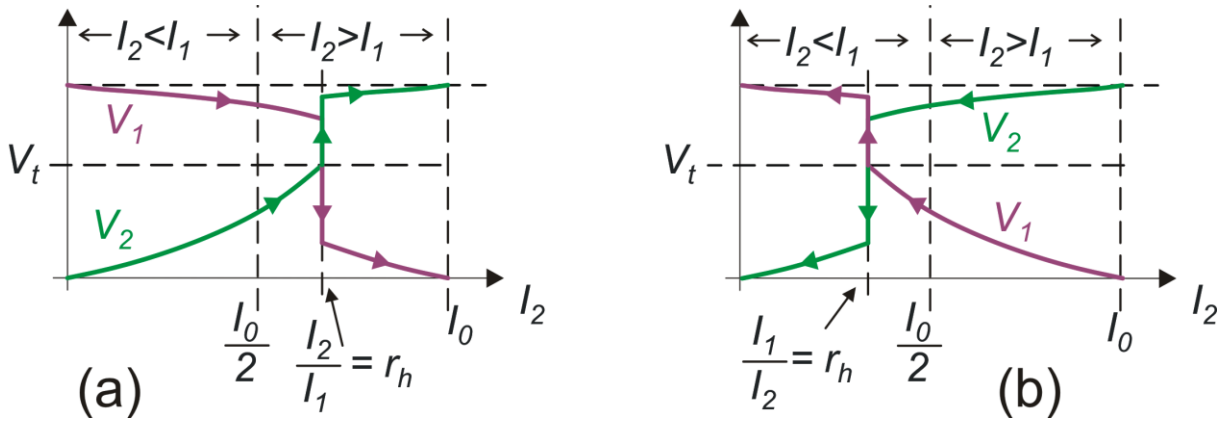

Fig.1.9. Dependence of V_1 and V_2 on I_2 when I_2 is increased from zero to I_0 (plot a) and decreased from I0 to zero (plot b).

Putting the two plots of Fig.1.9 together, we obtain the plot of Fig.1.10, which represents the full characteristic of the four-transistor hysteresis cell. Note that there is an interval of I_2 values around $I_0/2$ where two possible solution for the V_1,V_2 pair are possible. Which one of the solution is actually enforced depends of the previous history of the cell.

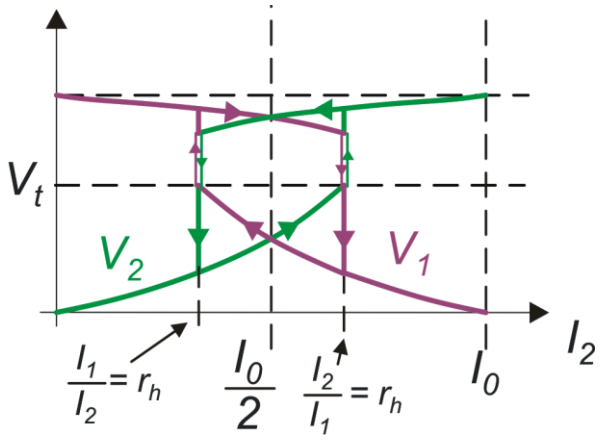

Fig.1.10. Complete characteristics of the four-transistor hysteresis cell.

It is possible to demonstrate the presence of the hysteresis also with different arguments. Let us consider the case I_1=I_2=I_0. Clearly, due to symmetry, a perfect symmetrical solution V_1=V_2 is possible. If we analyze the symmetrical solution, it can be easily demonstrated that all four transistors are active (on-state). For example, if we suppose that M1 is off, then also M4 should be off, because we are supposing that the solution is symmetrical. But V_{GS3}=V_{GS1} and V_{GS2}=V_{GS4}, thus, if M1 and M4 are both off, also M2 and M3 should be off and there is not a single MOSFET that carries I_1 and I_2. All four transistors should also be in saturation region, since, being V_1=V_2, the condition V_{GS}=V_{DS} applies to all of them. It is possible to divide the four-transistor cell (Fig.1.4) in two identical sub-circuits as shown in Fig.1.11. Each sub-circuit is equivalent to an amplifier where the small-signal gain is given by:

$$A = -g_{mC}\left(\frac{1}{g_{mL}} // r_{dC} // r_{dL}\right) \cong -\frac{g_{mC}}{g_{mL}} \tag{1.11}$$

The MOSFET output resistances r_{dC} and r_{dL} can be neglected in the parallel with respect to $1/g_{mL}$, since, in the symmetrical solution, all transistors are in saturation region where r_d>>1/gm. The four-transistor cell of Fig.1.4 is simply given by the connection of two sub-circuit as shown in Fig.1.12.

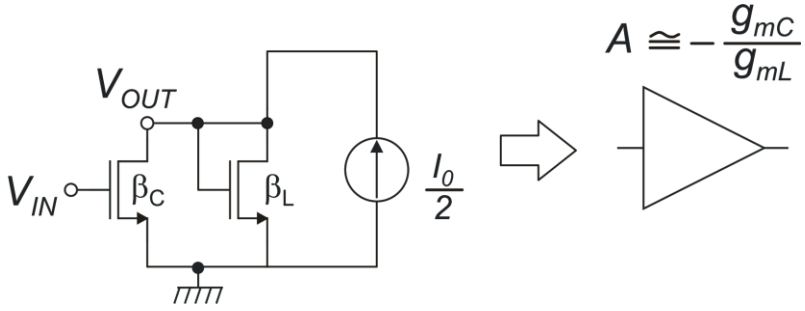

Fig.1.11. One of the two sub-circuit (amplifiers) which can be combined to form the four-transistor cell.

The representation of the cell given by Fig.1.12 is that of a feedback loop, with loop gain equal to A^2. Since the loop gain is positive in DC, if the modulus is positive, then the symmetrical solution is unstable.

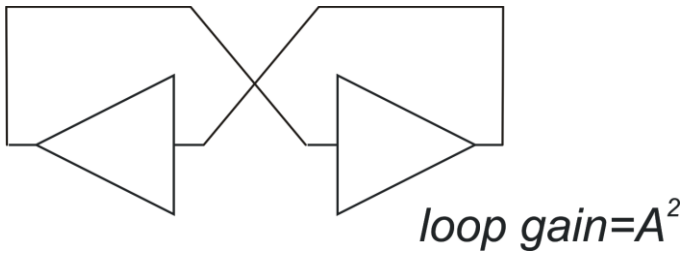

Fig.1.12. Connection of two sub-circuits of the type shown in Fig.1.11 to form the four-transistor cell. .

Since all transistors have the same V_{GS} (again, in the symmetrical solution), then, expressing g_m as $\beta(V_{GS}-V_t)$ equation (1.11) becomes:

$$A \cong -\frac{g_{mC}}{g_{mL}} = \frac{\beta_C}{\beta_L} \equiv r_h \tag{1.12}$$

Thus, if $r_h>1$ (i.e. $\beta_C>\beta_L$), as we have supposed when we have introduced condition (1.9), the symmetrical solution is not stable. Setting $I_1=I_2=I_0$, the symmetrical solution is a valid solution of the network equations, but if the circuit falls in that solution (for example at power-up time), it ends by collapsing into one of the two stable solutions shown in Fig.1.10, characterized by either $V_1>V_2$ or $V_1<V_2$. These solutions are stable because either V_1 or V_2 is below V_t, (see Fig.1.10), so that one of the two amplifiers of Fig. 1.12 is off, and the loop-gain is zero. Note that this analysis is in agreement with the arguments that led to Figs.1.9 (a) and (b): if $r_h>1$, then the transition occurs for $I_2>I_1$ when we proceed from the left to the right, and occurs at $I_2<I_1$ when we proceed from the right to the left.

On the other hand, if $r_h<1$, when with progressively increase I_2 from zero, V_2 reaches the threshold voltage V_t still in the region $I_2 < I_1$, Decreasing I_2 from I_0, V_1 reaches V_t in the region $I_2 > I_1$. Thus, in the center of the plot (around $I_2=I_0/2$), both V_1 and V_2 can be greater than V_t independently of the point we started from. This suggests that a hysteresis is not present, as confirmed by the fact that the loop-gain for $I_1=I_2=I_0/2$ is less than one, thus the symmetrical solution $V_1=V_2$ is stable. The curves for $r_h<1$ are shown in Fig. 1.13.

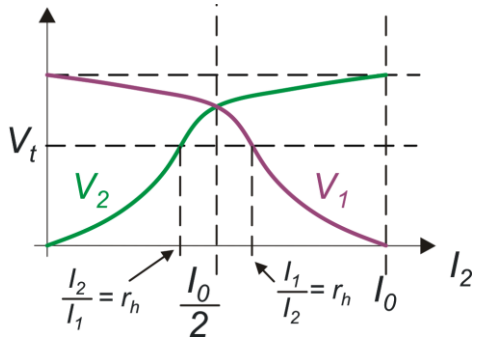

Fig.1.13. Response of the four-transistor cell for $r_h<1$ (i.e. $\beta_C<\beta_L$).

1.3 A simple regenerative comparator based on the four-transistor cell.

The cell in Fig.1.4 is marked by hysteresis when it is designed choosing r_h>1 (β_C>β_L). Unfortunately, it cannot be used as a comparator as it is, due to the following drawbacks:

1) Its inputs are currents (I_1 and I_2), while, in order to implement the function of Fig.1.3, the input should be a differential voltage.

2) The output voltages V_1 and V_2 are very far from being standard logical levels (such as 0 and V_{dd}).

However, considering the plots of Fig.1.9 (a) and (b) or the plot in Fig.1.10, we can verify the following property:

a) if we increase I_2 from from a region where I_2<<I_1, then V_1 > V_t and V_2<V_t up to the I_2 value such that I_2/I_1=r_h>1.

b) if we decrease I_2 from a region where I_2>>I_1, then V_2 > V_t and V_1<V_t down to the I_2 value such that I_2/I_1=1/r_h<1.

This means that in all possible stable states, there is only one diode-connected transistor (M1 or M4) to be active. This property is exploited to build a simple comparator capable of producing full logical level at the output port. The schematic view of this simple comparator is shown in Fig. 1.14.

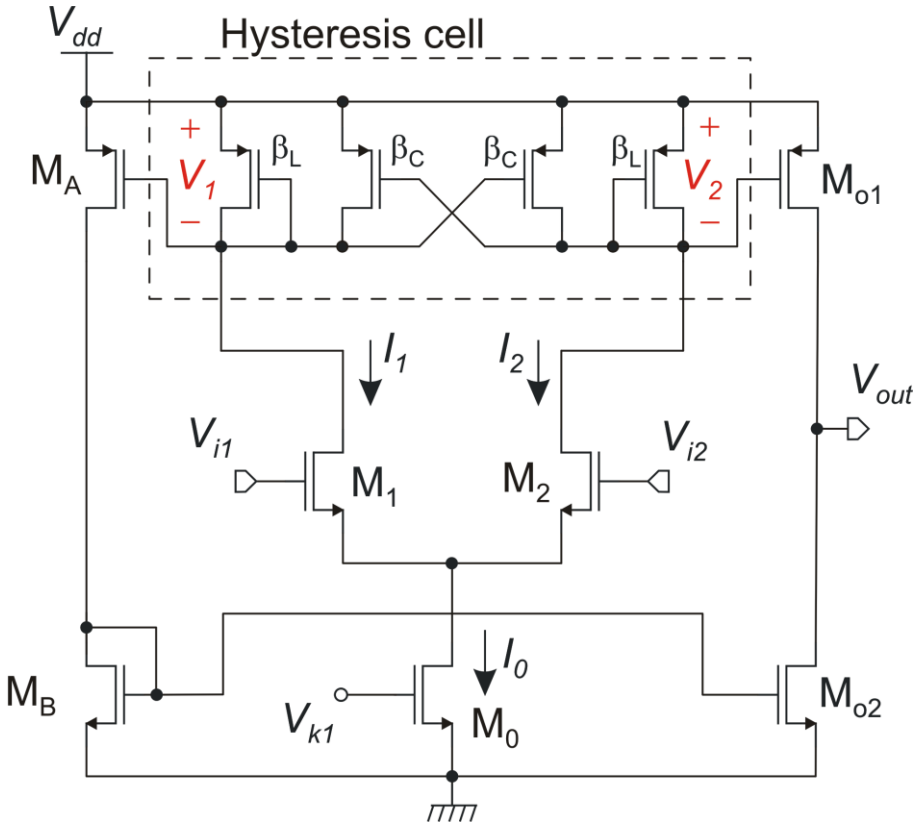

Fig.1.14. Schematic view of a simple comparator based on a p-type four-transistor hysteresis cell.

The circuit uses a p-version of the cell in Fig.1.4. Everything we have derived for the n-type cell is also valid for the p-type if we consider V_1 and V_2 referred to V_{dd} instead of ground, as shown in Fig.1.14. The output stage is formed by M_{01} and M_{02}. As far as M_{01} is concerned, it forms a current mirror with the diode transistor on the right. M_{02}, is driven by a current proportional to the current in M_A, which, in turn, forms a current mirror with the left diode transistor of the hysteresis cell. As a result, M01 is active only when the right diode transistor is active, M02 when the left diode is active. Then, M01 and M02 simply replicate the state (on or off) of the two diode-connected transistors of the hysteresis cell, respectively. Then only one out of Mo1 and M02 will be active. When M01 is active, it acts as a pull-up resistor and the output voltage is equal to Vdd (no path to ground is present, since M02 is off when M01 is on). When M02 is active it acts as a pull-down and no path to Vdd exists, so the the output voltage is zero. In this way, we have demonstrated that the only stable output voltages allowed are full logical levels.

Now let us consider that currents I_1 and I_2 are provided by the differential pair M1, M2, which are biased with a current I_0 by M0. Obviously the condition $I_1+I_2=I_0$ is satisfied. If we consider as the input differential voltage the difference:

$$V_d = V_{i2} - V_{i1} \tag{1.13}$$

we can write the following expressions for I_1 and I_2:

$$\begin{cases} I_2 - I_1 = g_{m1} V_{id} \\ I_2 + I_1 = I_0 \end{cases} \tag{1.14}$$

Imagine to apply a negative differential large enough to make $I_{D2}=0$. Then the hysteresis cell will be in the initial condition well described by conditions (1.3). The right diode connected transistor and M01 will be off, while M02 will be on. The output voltage is zero. Increase V_{id} we can increase I_{D2}, making the hysteresis cell go through the curves of Fig. 1.9 (a). The cell will change state for $I_2=r_H I_1$. Substituting this expression in (1.14), we find:

$$\frac{I_2 - I_1}{I_2 + I_1} = \frac{r_H - 1}{r_H + 1} = \frac{g_{m1}}{I_0} V_H \tag{1.15}$$

where V_H indicates the upper threshold of the comparator (see Fig.1.3). Considering that in rest conditions ($V_{id}=0$), $I_0=2I_{D1}$, then $g_{m1}/I_0=1/2V_{TE1}$, so that:

$$V_H = 2V_{TE1} \frac{r_H - 1}{r_H + 1} \tag{1.16}$$

where V_{TE1} is the equivalent thermal voltage of the MOSFET calculated in the rest condition. It can be easily shown that, due to symmetry, the negative threshold V_L is equal to $-V_H$, so that the total hysteresis range is equal to:

$$\Delta V_h = 2V_H = 4V_{TE1} \frac{r_H - 1}{r_H + 1} \tag{1.17}$$

In strong inversion, we have $V_{TE}=(V_{GS}-V_t)/2$, so that:

$$\Delta V_h = 2\left(V_{GS} - V_t\right)_1 \frac{r_H - 1}{r_H + 1} \qquad \text{(strong inversion)} \tag{1.18}$$

1.4 Comparators with very low hysteresis.

There are several cases where the hysteresis range should be very small. For example, if the comparator has to be used in an ADC, the hysteresis should be smaller than the LSB, which, for high-resolution converters can be in the order of several tens of microvolts. The circuit of Fig.1.14 is unable to reach such small hysteresis levels. To understand this, equation (1.17) can be taken into account. Voltage V_{TE1} can be made as small as nearly 30-40 mV pushing M1 and M2 in weak inversion. This value should be reduced by at least three orders of magnitude. In principle, this could be done by choosing r_h very close to one, in order to minimize the numerator (r_h-1). In practice, r_h should be kept well greater than one to avoid that process errors and systematic errors due to approximate analysis [e.g. due to neglecting r_{dC} and r_{dL} in (1.11)] cause the loop gain to drop below unity, cancelling the hysteresis. Furthermore, it can be demonstrated that the larger rh, the smaller the transition time. A typical case is r_h=2, leading to an hysteresis range equal to $\Delta V_h = 4V_{TE1}/3$, which, for what we have seen before, is of the order of several tens millivolts.

In order to obtain very small hysteresis ranges, the optimum approach is to place a pre-amplifier before the regenerative comparator, as shown in Fig.1.15. It can be easily shown that the composite comparator of Fig.1.16 has a hysteresis range $\Delta V_{h\text{-}RTI}$ given by:

$$\Delta V_{h-RTI} = \frac{\Delta V_h}{G} \tag{1.19}$$

where ΔV_h is the hysteresis width of the original regenerative comparator, while G is the gain of the pre-amplifier. With G in the order of a several thousands, the effective hysteresis range can be easily reduced to a few microvolts.

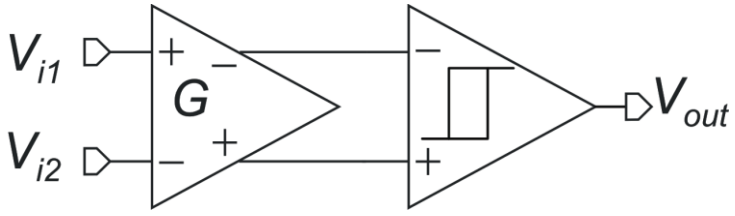

Fig.1.15. Schematic view of a simple comparator based on a p-type four-transistor hysteresis cell.

In these conditions, the main source of error is the offset of the pre-amplifier, which is generally a few millivolts or higher. Such an offset is not acceptable when the comparator is used in precision ADCs. In those cases, it is possible to cancel the offset by means of correlated double sampling. The principle is shown with the simple but effective circuit of Fig.1.16. In phase 1, the amplifier is closed in unity gain configuration, so that its input signal is very close to the offset voltage. This voltage is stored across the two input capacitors. In phase two, the amplifier operates in open loop configuration, delivering its full gain G. The offset voltage, stored into the input capacitors, is added to the input

signal, obtaining a virtually offset-free amplifier. Clearly, the output of the comparator is valid only in phase 2.

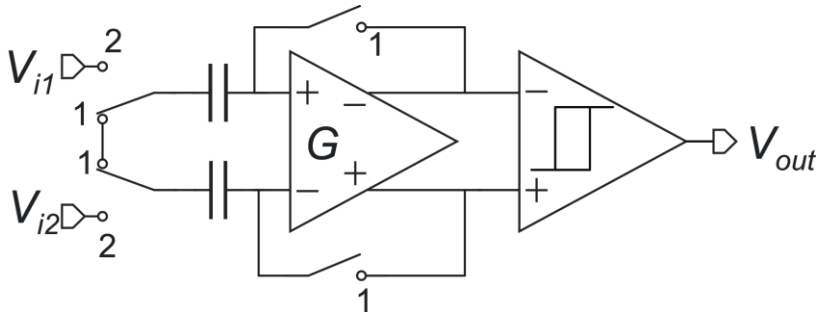

Fig.1.16. Cancellation of the pre-amplifier offset by means of correlated double sampling.

1.5 A simple low frequency VCO based on a regenerative comparator.

There are applications where a very wide hysteresis range is desirable. Examples of these applications are relaxation oscillators. A relaxation oscillator is a circuit where a memory element (typically a capacitor but also an inductor can be used) is charged up to a given value (upper threshold) and then discharged to a lower value (lower threshold). Relaxation oscillators produce non-sinusoidal waveforms such as square, triangle or saw-tooth signals. All modern microcontroller includes one or more relaxation oscillators, which are used to provide clock signals with no need of a quartz crystal. Their frequency accuracy is generally poor, but can be significantly improved if frequency trimming is used. For example, various microcontroller families use relaxation oscillations that are factory-trimmed to reduce frequency error and temperature drift to values as low as to be acceptable in commonly used communication standards (e.g. UART serial communication).

A simple relaxation oscillator, based on a regenerative comparator, is shown in Fig. 1.17. Devices Mp and Mn operates as switches that connect capacitor C to the current source I_P (charge current) when V_{out} is low and to I_N (discharge current) when V_{out} is high.

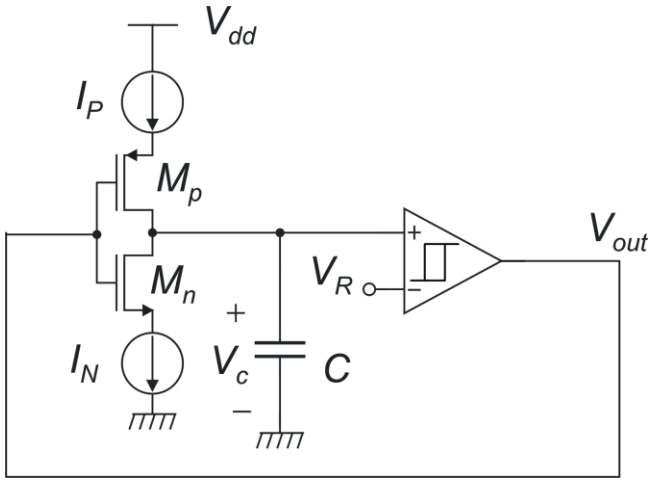

Fig.1.17. A simple relaxation oscillator based on a regenerative comparator.

A constant voltage V_R is applied to the inverting terminal of the comparator. Thus, we can define two threshold voltages, V_{SET} and V_{RES} (set and reset, respectively, $V_{SET} > V_{RES}$) for V_C, given by:

$$V_{SET} = V_R + V_H = V_R + \frac{\Delta V_h}{2}$$
$$V_{RES} = V_R - V_H = V_R - \frac{\Delta V_h}{2} \qquad (1.20)$$

When $V_C < V_{RES}$, V_{out} is low, while if $V_C > V_{SET}$, V_{out} is high, regardless of the previous history of the circuit. If V_{out} is low, it needs to reach V_{SET} to be turned high, while it should go down to V_{RES} to be turned low, when starting from a high state. This behavior is clearly a consequence of the hysteresis. We will suppose than V_R is such that $V_{RES} > 0$. If this condition is verified, clearly also V_{SET} is positive.

We can start by considering an initial condition where V_C starts from zero. For what we have stated above, V_{out} is certainly low. Then, I_P is connected to the capacitor and V_C is progressively increased in a linear fashion, with a slope (time derivative) equal to I_P/C. The relevant waveforms are shown in Fig. 1.18.

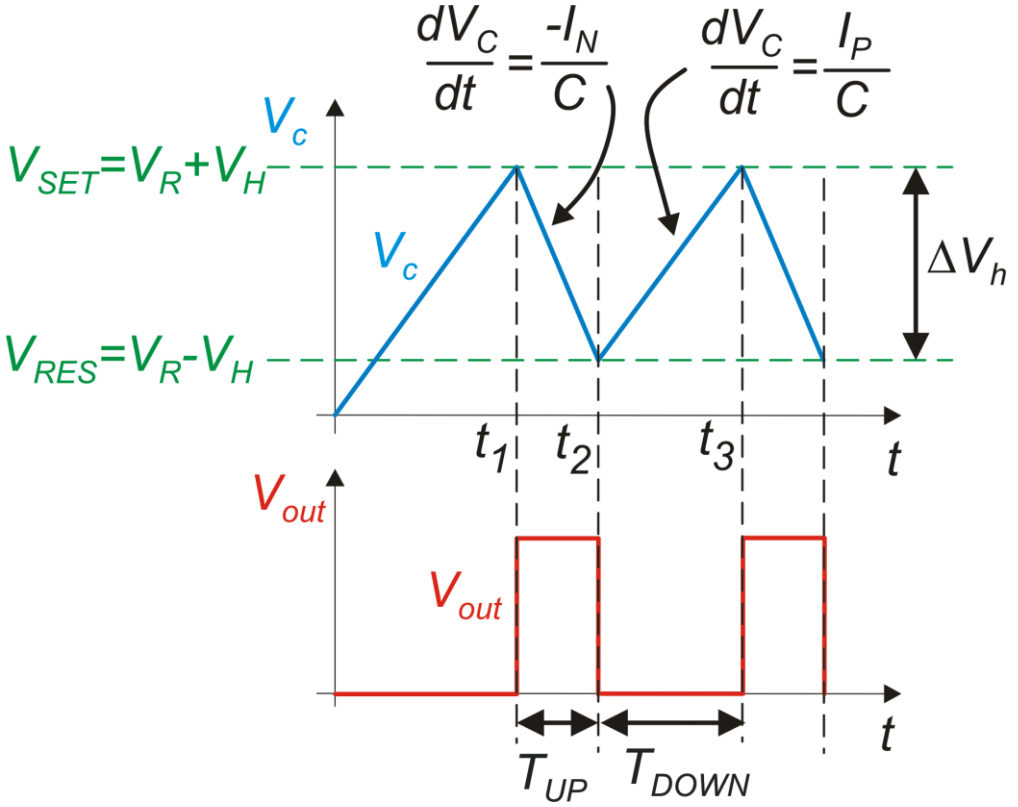

Fig.1.18. A simple relaxation oscillator based on a regenerative comparator.

When V_C reaches the lower threshold V_{RES}, nothing happens since it is already low. In order to turn V_{out} high it is necessary for V_C to reach V_{SET}. When it happens (time t_1), Mn turns on while Mp is switched off, so that I_N starts discharging capacitor C, making V_C decrease with a slope given by $-I_N/C$. When V_C

reaches the lower threshold V_{RES}, the output voltage turns low again (time t_2) and V_C is increased again with a slope I_P/C. until V_{SET} is reached at time t_3. After this time, the waveforms repeat periodically. Note that V_C oscillates between the two thresholds V_{RES} and V_{SET}, with a charging interval of duration T_{DOWN} (V_{out}=0) and a discharge period of duration T_{UP} (V_{out}=1). These times are given by the total voltage variation, which in both cases is given by the hysteresis range ΔV_h, divided by the respective slopes, according to:

$$\begin{aligned} T_{UP} &= \frac{\Delta V_h}{I_N / C} = C\frac{\Delta V_h}{I_N} \\ T_{DOWN} &= \frac{\Delta V_h}{I_P / C} = C\frac{\Delta V_h}{I_P} \end{aligned} \tag{1.21}$$

Caring the ratio between I_P and I_N, it is possible to change the duty cycle of the output rectangular waveform (V_{out}). If I_P=I_N=I_{TUNE}, T_{UP} and T_{DOWN} are identical and V_{out} becomes a square waveform with 50 % duty cycle. In this condition, the waveform period T= T_{UP}+T_{DOWN} is given by:

$$T = 2C\frac{\Delta V_h}{I_{TUNE}} \tag{1.22}$$

while the frequency, f=1/T is:

$$f = 2\frac{I_{TUNE}}{\Delta V_h C} \tag{1.23}$$

We have obtained an oscillator whose frequency is proportional to the tuning current I_{TUNE}. In order to obtain I_N and I_P from a single input current, the circuit in Fig. 1.19 can be used.

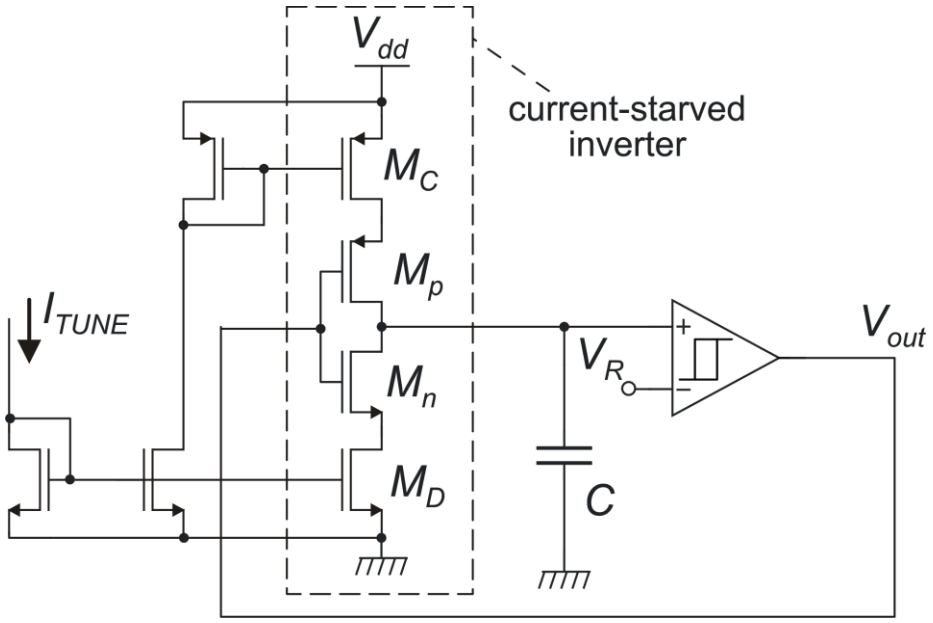

Fig.1.19. Implementation of the circuit of Fig.1.17 by means of a current-starved inverter.

The current sources providing I_N and I_P are replaced by M_D and M_C MOSFETs, respectively, whose current is set by means of a series of mirrors. Note that the structure of Mp and Mn is that of a digital CMOS inverter. In a standard CMOS inverter, Mp and Mn sources are connected to Vdd and gnd, respectively, so that the maximum output current supplied by the inverter is limited only by the device aspect ratio. In the inverter of Fig.1.19, the output current is limited by M_D and M_C current sources. For this reason, this kind of inverter is named "current-starved inverter". Devices M_D and M_C are the output branches of current mirrors that makes both I_P and I_N proportional to I_{TUNE}. The current gain of the mirrors can be designed to choose the desired I_P/I_N ratio, setting in this way the duty-cycle of the output waveform. If a 50 % duty-cycle it is possible to design the current mirrors to make $I_N=I_P=I_{TUNE}$, leading to equations (1.22) and (1.23).

In order to obtain a real VCO, where the frequency is controlled by a voltage, it is possible to use the simple Voltage-to-Current (I-to-V) linear converter shown in Fig.1.20.

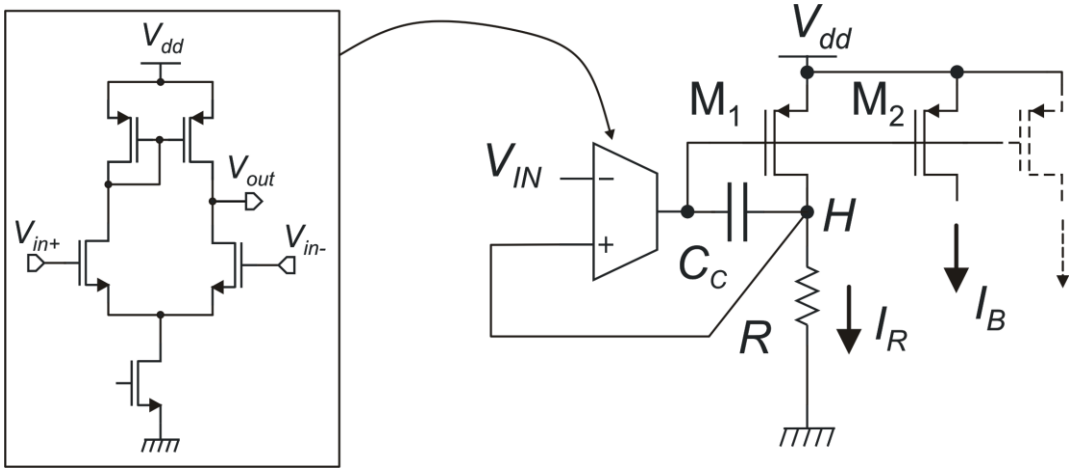

Fig.1.20. Simple versatile voltage to current converter.

The input differential amplifier can be implemented by means of the simple circuit shown on the left. The cascade of the amplifier and M1 (loaded by resistor R) forms an operational amplifier whose output port is node H. This composite op-amp is closed in unity gain configuration, so that $V_H=V_{IN}$. Note that, since M1 form an inverting stage (common source), the inverting input of the composite op-amp is the non-inverting input of the differential amplifier. Current through R is then V_{IN}/R. This current is carried by M1, which shares the same V_{GS} with M2, so that the output current I_B is given by:

$$I_B = \frac{V_{IN}}{R}\frac{\beta_2}{\beta_1} \tag{1.24}$$

It is possible to add other MOSFETS like M2, obtaining other currents all of which are proportional to VIN. The aspect ratio of the additional transistors can be made different from that of M2, if different currents are required. The circuit in Fig. 1.20 can be used, for example, to obtain constant bias current from a reference voltage VIN produced by a Band-Gap circuit. In this way it is possible to obtain all the currents that are required to bias complex analog circuits. The currents produced by the circuit in

Fig.1.20 are all positive (sourcing), but can easily transformed in negative (sinking) currents by means of n-type current mirrors.

Coming back to the VCO, we can use the circuit in Fig.1.20 to convert a tuning voltage V_{TUNE} into the tuning current I_{TUNE}. In this case, the relationship between the oscillator frequency and V_{TUNE} becomes:

$$f = 2\frac{V_{TUNE}}{\Delta V_h}\frac{1}{CR}\frac{\beta_2}{\beta_1} \tag{1.25}$$

Note that we have an inverse proportionality to capacitance C and R. This can be used to build a simple capacitance-to-frequency converter or a resistance-to-frequency converter, when V_{TUNE} is kept constant. In this way, simple interfaces for capacitive or resistive sensors can be designed. Note that a frequency signal can be easily converted into a digital code by counting the number of cycles over a given time window, or measuring the period of the waveform, by means of a similar method.